In the Specification

Please substitute the following annotated paragraph for paragraph [015] (beginning on page 6, line 11)

Fig. 1 is a circuit diagram of a pixel 10 of an electroluminescence ("EL") device in accordance with one embodiment of the present invention. The EL device consistent with the present invention includes a plurality of scan lines, a plurality of data lines, an array of pixels, a scan driver (not shown) sequentially providing a voltage signal having a first state S_{11} and a second state S_{12} to select the scan lines, and a data driver (not shown) sequentially providing a current signal I_{DATA} to the data lines. In one embodiment according to the invention, the EL device includes an organic EL device, which may further include an organic light emitting diode ("OLED") or a polymer light emitting diode ("PLED"). A difference between an OLED and a PLED lies in the size of light emitting molecules used in a light emitting layer. The light emitting molecules of an OLED are smaller than those of a PLED.

Please substitute the following annotated paragraph for paragraph [019] (beginning on page 8, line 6)

During a write stage, or in response to the first state S_{11} of the voltage signal provided over scan line 12, fifth transistor 30 and second transistor 22 are turned on. Current signal I_{DATA} is provided over data line 14 to pixel 10. Third transistor 26, operating in a saturation mode, is turned on to provide a first current equal to I_{DATA}. Fourth transistor 28 is turned on because gate electrode 28-2 is biased at a same voltage level as gate electrode 26-2 of third transistor 26. Since second transistor 22 is turned on, capacitor 24

is charged by a drain current (not shown) of second transistor 22, providing a voltage level V_C across capacitor 24 or across first electrode 20-4 and gate electrode 20-2, which turns on first transistor 20. As a result, a first current I_{DATA} flows through first transistor 20, third transistor 26 and fifth transistor 30 to data line 14. A second current equal to 1/N I_{DATA} flows through first transistor 20 and fourth transistor 28 to LED 32. Since a total of (1 + 1/N) I_{DATA} current flows through first transistor 20, voltage level V_C must satisfy the following equation.

Please substitute the following annotated paragraph for paragraph [022] (beginning on page 9, line 1)

During a reproducing stage, or in response to the second state S_{12} of the voltage signal, fifth transistor 30 and second transistor 22 are turned off. The voltage level across capacitor 24 during the write stage is maintained at V_C, which turns on first transistor 20. A third current (shown in a dotted line) equal to approximately (1 + 1/N) I_{DATA} from first transistor 20 turns on fourth transistor 28 and flows to LED 32. In one embodiment according to the invention, first power supply V_{DD} provides a voltage level ranging from approximately 7V (volts) to 9V, second power supply V_{SS} provides a voltage level ranging from approximately -8V to -6V. The voltage signal ranges from approximately -6V to 8V. The current signal ranges from approximately 1 μA (microampere) to 2 μA.

Please substitute the following annotated paragraph for paragraph [023] (beginning on page 9, line 11)

In view of the above, in response to the first state S_{11} of the voltage signal, first circuit 16 provides voltage level V_C across capacitor 24, and second circuit 18 provides second current 1/N I_{DATA} flowing thru LED 32. In response to the second state S_{12} of the voltage signal, first circuit 16 maintains voltage level V_C, and provides third current (1 + 1/N) I_{DATA} flowing thru LED 32.

Please substitute the following annotated paragraph for paragraph [025] (beginning on page 9, line 22)

Fig. 2 is a circuit diagram of a pixel 50 of an electroluminescence ("EL") device in accordance with another embodiment of the present invention. Pixel 50 has a similar circuit structure to pixel 10 shown in Fig. 1 except that transistors are NMOS transistors. Pixel 50 includes a first circuit 56 and a second circuit 58. First circuit 56 further comprises a first transistor 60, a second transistor 62, and a capacitor 64. Second circuit 58 further comprises a third transistor 66 and a fourth transistor 68. Pixel 50 further comprises a fifth transistor 70 and an LED 72. In response to a first state S_{21} of a voltage signal provided over a scan line 52, first circuit 56 provides a voltage level V_C across capacitor 64, resulting in a first current I_{DATA} flowing from a data line 54 through transistors 70, 66 and 60, and second circuit 58 provides a second current 1/N I_{DATA} flowing thru LED 72. In response to a second state S_{22} of the voltage signal, first circuit 56 maintains voltage level V_C, and provides a third current (1 + 1/N) I_{DATA} flowing thru LED 72.

Please substitute the following annotated paragraph for paragraph [027] (beginning on page 10, line 18)

The present invention also provides a method of operating an electroluminescence device. A voltage signal having a first state S_{11} and a second state S_{12} is provided. A current signal having a magnitude I is provided. An array of pixels 10 is provided. Each of pixels 10 is disposed near an intersection of one of scan lines 12 and one of data lines 14. Each of pixels 10 is provided with a first circuit 16 including a first transistor 20, a second transistor 22 and a capacitor 24. A voltage level V_C across capacitor 24 is provided in response to the first state S_{11} of the voltage signal provided over a corresponding scan line 12. Voltage level V_C is maintained in response to the second state S_{12} of the voltage signal. Each of pixels 10 is provided with a second circuit 18 including a third transistor 26 and a fourth transistor 28. Third transistor 26 includes a gate electrode 26-2 coupled to a gate electrode 28-2 of fourth transistor 28. A first current of (1 + 1/N) I is provided from first circuit 16 during the second state S_{12} of the voltage signal. A second current of (1/N) I is provided from second circuit 18 in response to the first state S_{11} of the voltage signal, N being the ratio of a channel width/length of third transistor [[16]] 26 to that of fourth transistor [[18]] 28.

Please substitute the following annotated paragraph for paragraph [028] (beginning on page 11, line 11)

The method further comprises providing a fifth transistor 30 including a gate electrode 30-2 receiving the voltage signal, and an electrode 30-4 receiving the current signal. The method further comprises providing a light emitting diode 32. In one embodiment according to the present invention, first current of (1 + 1/N) I is provided ~~to LED 32~~ during the first state of the voltage signal. In another embodiment, first current of

(1 + 1/N) I is provided ~~to LED 32~~ during the second state of the voltage signal. In still another embodiment, second current of (1/N) I is provided during the first state of the voltage signal. In yet still another embodiment, second current of ~~(1/N)~~ (1 + 1/N) I is provided during the second state of the voltage signal.